

INTERNATIONAL PRELIMINARY EXAMINATION REPORT
(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P-2002-012WO	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/DK 03/00339	International filing date (day/month/year) 22.05.2003	Priority date (day/month/year) 07.06.2002
International Patent Classification (IPC) or both national classification and IPC H01L21/302		
Applicant OTICON A/S et al.		

<p>1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of 6 sheets, including this cover sheet.</p> <p><input type="checkbox"/> This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of sheets.</p>
<p>3. This report contains indications relating to the following items:</p> <ul style="list-style-type: none"> I <input checked="" type="checkbox"/> Basis of the opinion II <input type="checkbox"/> Priority III <input type="checkbox"/> Non-establishment of opinion with regard to novelty, inventive step and industrial applicability IV <input type="checkbox"/> Lack of unity of invention V <input checked="" type="checkbox"/> Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement VI <input type="checkbox"/> Certain documents cited VII <input type="checkbox"/> Certain defects in the international application VIII <input type="checkbox"/> Certain observations on the international application

Date of submission of the demand 06.01.2004	Date of completion of this report 01.09.2004
Name and mailing address of the International preliminary examining authority:  European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Cockcroft, Y Telephone No. +49 89 2399-2436
	

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I. Basis of the report

1. With regard to the **elements** of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17)*):

Description, Pages

1-12 as originally filed

Claims, Numbers

1-10 as originally filed

Drawings, Sheets

1/2-2/2 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- the language of publication of the international application (under Rule 48.3(b)).
- the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- contained in the international application in written form.
- filed together with the international application in computer readable form.
- furnished subsequently to this Authority in written form.
- furnished subsequently to this Authority in computer readable form.
- The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- the description, pages:
- the claims, Nos.:
- the drawings, sheets:

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5. This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).
(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	1-10
	No: Claims	
Inventive step (IS)	Yes: Claims	
	No: Claims	1-10
Industrial applicability (IA)	Yes: Claims	1-10
	No: Claims	

2. Citations and explanations

see separate sheet

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To Point V

Reference is made to the following documents:

D1 = US-A-5 244 537; and

D2 = US-A-5 591 665.

A via is also known as a through hole such that formation of a through hole in a substrate is to be considered as defining a via in said substrate. However, claim 1 details the formation of a through-hole followed by defining of the via. The verb "to define" has the meaning "to determine the boundary or extent of" or "to delineate the form or outline of" (Collins English dictionary). Since a via is a through hole the step of defining the via can only be considered as a step of forming this via. It is thus not apparent whether "the via" is the same as "the feed-through" of claim 1 and how the defining of the via differs from the generation of the through-hole. The feature of claim 1 that subsequent to formation of the through-hole the via is defined is not clear and claim 1 fails to satisfy Article 6 PCT in this respect.

The applicant has referred to the step of forming an electrically conducting path running through the hole and on both sides of the wafer, which step does indeed require a photomasking step. This step is however not a step of "defining" the via, but is a step of rendering the via **and certain areas on the wafer surfaces** conducting. Thus an amended claim 1 indicating that in the final step "a photomasking step is subsequently used to coat the via and areas on the front side and back side of the wafer with metal" would satisfy Article 6 PCT.

Document D1 shows a process for generating a feed-through in a semiconductor wafer, which has electric circuitry on a front surface thereof, whereby the hole for the feed-through is generated by the combined use of a front side protection layer and a wet KOH etch process etching the hole from the back side of the wafer (see figures 3a and 1b and column 3, line 57 to column 4, line 64).

Thus the method of D1 differs from that of claim 1 in that the circuitry is on the substrate rather than in it and in that material is not deposited in the through-hole after formation. Clearly the positioning of the circuitry depends on the exact device required and the skilled person will place circuitry within the substrate when forming devices such as transistors etc. as this is the normal way of producing these type of devices. Document D2 clearly shows a structure with electrical circuitry embedded in a front

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surface thereof (see figure 1 and the corresponding text), such that this difference is known in the prior art. Moreover, whether material is deposited in the via after formation also depends entirely on the purpose of the via. When this is intended to be used to contact one side of the substrate to the other, it will be routine for the skilled person to deposit metal in the via and he will do this without the need for any inventive thought.

Claim 1 lacks inventive merit compared to the teaching of D1 and D2 and the routine knowledge and capabilities of the skilled person. Article 33.3 PCT is not satisfied.

The applicant has indicated that D1 does not refer to delicate circuitry such as CMOS circuits and that this is an important feature of the claimed method. However, these arguments cannot be taken into consideration as claim 1 of the application is not restricted to such circuitry, but allows the selection of any electric circuitry. These arguments are thus not relevant to the claim as currently on file.

However, even were claim 1 to be restricted to CMOS type circuitry, an inventive step could not be recognised as D2 clearly discloses such circuitry, along with etching of the back face of the wafer using KOH (column 3, line 16-32). The applicant's argument that it is not known to etch delicate circuitry using KOH with only a frontside protection layer on the wafer is therefore not accepted. D2 explicitly discloses etching with KOH wherein either no protection is used, or a layer of protective polyimide is used on the front face of the wafer (column 3, lines 28-32). Thus even an amended claim 1, which contained those features which the applicant suggests are crucial to the invention, but which are currently absent from claim 1, would not be sufficient to render claim 1 inventive over the teaching of D1 and D2.

The front side protection layer of D1 comprises a silicon nitride layer and claim 2 also lacks inventive merit.

The features of claim 3 are all explicitly seen in D1 with the exception of the use of a photomasking process to form the through-holes in the nitride layer. D1 is silent as to how this layer is patterned, but photomasking is the standard way to pattern a masking layer and the skilled person will consider this as the first possibility when reading D1. Claim 1 cannot render preceding claims inventive compared to the prior art.

There are only two alternative ways to etch the layers on the front of the substrate, either from the front (as in D1) or from the back, through the through-hole once this is

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formed. The skilled person will select the preferred alternative without any inventive skill being required. Claims 4 and 5 do not satisfy the requirements of Article 33.3 PCT.

It is common practice to line via holes and when they are to be coated by electroplating then clearly a plating base is also required. Claim 6 contains only features which will readily be considered by the skilled person.

Dependent claims 7-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, as they detail only standard steps utilised when required during device fabrication.

Once the skilled person is aware from D1 and his own knowledge that he can form feed-throughs using etching in KOH he will readily apply this technology to the formation of amplifiers. Independent claim 10 does not appear to contain any features which could be considered as requiring inventive thought such that the requirements of Article 33.3 are not met.